REMARKS

The present amendment is submitted in response to the Office Action mailed September 30, 2008. In view of the amendments above and the remarks to follow, reconsideration and allowance of this application are respectfully requested.

Applicant thanks the Examiner for indicating that the drawings filed on 20 April, 2006 are acceptable.

Claim Status

Claims 1-13 remain in this application. Claims 1-11 have been amended. New Claims 12 and 13 have been added. The claims in general are amended for one or more non-statutory reasons, for example to correct one or more informalities or obvious errors, remove figure label number(s), remove unnecessary limitations, and/or replace European claim phraseology with U.S. claim language having the same meaning. The claims are not believed to be narrowed in scope and no new matter is added.

Claim Objections

The Office objects to claims 1, 3, 5, and 8-11 because of the following informalities. With particular reference to claims 1, 9 and 10, each of these claims stands objected for reciting the term "*prohibiting the provision and/or the output*", which the Office asserts lacks antecedent basis. In response, Applicant has amended claims 1, 9 and 10 in a manner which is believed to overcome the objections.

With particular reference to claims 3, 5, 8 and 9, the Office objects to these claims for reciting the term, "*in particular*", which renders the claims unclear. Applicant has amended claims 3, 5, 8 and 9 in a manner which is believed to overcome the objections.

With particular reference to claim 10, the Office objects to this claim due to an informality. Specifically, the term "*said integrated circuit*" lacks antecedent basis.

Applicant has amended claim 10 in a manner which is believed to overcome the objection.

Rejections under 35 U.S.C. §101

Claim 11 stands rejected under 35 U.S.C. §101 as being allegedly directed to non-statutory subject matter. As per claim 11, the rejection is understood to be based on the premise that the claim is directed to a computer program which does not fall within a statutory category of invention. The Office further states that the program is not stored on any computer readable storage medium, nor is any computer readable storage medium disclosed in the specification as storing such program or code.

In response, Applicant has amended claim 11 in a manner which is believed to overcome the rejection. Support for the amendment can be found, for example, at page 3 of the specification which recites, "*. A computer program for implementing said method **on a computer** is defined in claim 11."* Accordingly, withdrawal of the rejection is respectfully requested.

Rejections under 35 U.S.C. §102(b)

In the Office Action, Claims 1-6 and 8-11 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,757,832 ("Silverbrook"). Applicant respectfully traverses the rejection.

A. Claims 1-6 and 8 are allowable

The cited portions of Silverbrook do not anticipate claim 1 because the cited portions of Silverbrook do not teach every element of claim 1. For example, the cited portions of Silverbrook do not disclose or suggest, "*a delay means comprising an analog noise source for adding a noise signal to the response data signal provided by said response signal providing means, the delay means for delaying and/or prohibiting a*

provision and/or the output of said response data signal", as recited in claim 1 (Emphasis Added). In contrast to claim 1, the cited portions of Silverbrook disclose a digital noise source implemented for a different purpose and in a different manner than taught by the invention and as recited in claim 1. Silverbrook discloses the use of a linear feedback shift register (LFSR), not for the purpose of delaying or hindering normal chip read-out, but instead, for encryption purposes (i.e., to prohibit or thwart the breaking of the chip's contents) via externally monitoring internal digital chip activity (e.g., by monitoring the supply current or the emitted radio frequency energy).

See, Silverbrook at col. 81, lines 3-15.

"*...Each authentication chip should contain* ***a noise generator*** *that generates continuous circuit noise.* ***The noise will interfere with other electromagnetic emissions from the chip's regular activities*** *and* ***add noise to the Idd signal.*** *Placement of the noise generator is not an issue on an authentication chip due to the length of the emission wavelengths. The noise generator is used to generate electronic noise, multiple state changes each clock cycle, and as a source of pseudo-random bits for the Tamper Prevention and Detection circuitry (see Section 10.1.5).*" (Emphasis Added).

Silverbrook further discloses that an SEPM attack can be simply thwarted by adding a metal layer to cover the circuitry. However an attacker could etch a hole in the layer, so this is not an appropriate defense. To overcome such an attack, Silverbrook discloses the use of Tamper Detection circuitry that shields an emanating signal as well as cause circuit noise. The noise produced by the circuit of Silverbrook will actually be a greater signal than the one that the attacker is looking for. If the attacker attempts to etch a hole in the noise circuitry covering the protected areas, the chip will not function, and the SEPM will not be able to read any data. Thereby making an SEPM attack fruitless. Applicant submits that utilizing Tamper Prevention and Detection Circuitry for the

purpose of delaying and/or prohibiting a provision and/or the output of said response data signal", as recited in claim 1.

Silverbrook teaches that a Noise Generator causes circuit noise to interfere with other electromagnetic emissions from the chip's regular activities and thus obscure any meaningful reading of internal data transfers. *See* Silverbrook, col. 87, lines 61-67 through col. 88, lines 1-14. It is respectfully submitted that encryption protection via the blockage of electromagnetic emissions to obscure meaningful readings of internal data transfers is different than utilizing analog delay means for the purpose of delaying and/or prohibiting the provision and/or the output of a data response signal, as recited in claim 1.

See Silverbrook, col. 88, lines 15-19:

"*The Noise Generator circuit (which also acts as a defense against EMI attacks) will also cause enough state changes each cycle to obscure any meaningful information in the Idd signal.*"

It is further submitted that the noise generator of Silverbrook is implemented by digital means in contrast to the analog noise generator, recited in claim 1.

See, Silverbrook, col. 81, lines 15-18.

"*A simple implementation of a noise generator is a* ***64-bit maximal period LFSR*** *seeded with a non-zero number. The clock used for the noise generator should be running at the maximum clock rate for the chip in order to generate as much noise as possible.*"

Thus, the cited portions of Silverbrook do not disclose or suggest, "*a delay means comprising an analog noise source for adding a noise signal to the response data signal provided by said response signal providing means, the delay means for delaying and/or prohibiting a provision and/or the output of said response data signal*", as recited in claim 1 (Emphasis Added). Thus, claim 1 is allowable.

Claims 2-6 and 8 are allowable at least by virtue of their dependence from claim 1.

Further, dependent claim 6 recites additional features that are not disclosed or suggested by the cited portions of Silverbrook. For example, the cited portions of Silverbrook do not disclose an information Information carrier, wherein said delay means comprise analog limiting means for restricting the number of response data signals provided and/or outputted per time unit.

B. Claims 9-11 are allowable

Independent claims 9 and 10 recite similar subject matter as claim 1, and are allowable for at least the same reasons as provided above for claim 1. Claim 11 is allowable at least by virtue of its dependence from claim 10.

Rejections under 35 U.S.C. §103

In the Office Action, Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Silverbrook, and further in view of U.S. Patent No. 7,120,808 ("Miyaira"). Applicant respectfully traverses the rejection.

As explained above, the cited portions of Silverbrook do not disclose or suggest each and every element of claim 1, from which claim 7 depends. Miyaira does not disclose each of the elements of claim 1 that are not disclosed by Silverbrook. For example, Miyaira does not disclose or suggest "*a delay means comprising an analog*

noise source for adding a noise signal to the response data signal provided by said response signal providing means, the delay means for delaying and/or prohibiting a provision and/or the output of said response data signal", as recited in claim 1 (Emphasis Added). Instead, the cited portions of Miyaira disclose limiting the amount of power available per unit time. See Miyaira, col. 7, lines 55-67 and col. 10, lines 14-31). Therefore, claim 1 is allowable over the asserted combination of Silverbrook and Miyaira, and claim 7 is allowable, at least by virtue of its dependence from claim 1.

New Claims

New claim 12 has been added to further clarify claim 3. Namely, new claim 12 recites that the signal generation means recited in claim 3 is an encryption unit.

New claim 13 has been added, as an independent claim, to further clarify claim 5. Namely, claim 13 recites that the delay means comprises a noisy read-out amplifier for amplifying the response signal provided by said response signal providing means. Applicant respectfully submits that the analog approaches taught by the invention are far more robust than the digital methods taught in Silverbrook. That is, after contemplating a digital approach, the inventor has concluded that it would be easier to reverse engineer a chip that utilizes digital delay means by having an understanding of the chip construction. The inventor therefore elected to take an analog approach for implementing delay means. In one approach, a noisy read-out amplifier is used to amplify a response signal. The noise produced by such a noisy amplifier is based on the physics of the device and as such is indiscernible. In other words, one cannot reverse engineer the noise produced by a noisy read-out amplifier, but one can reverse engineer artificial digital noise from a device, as taught in Silverbrook. It should be appreciated that the second analog approach for providing delay means is recited in claim 1 with regard to the recited analog noise source for adding a noise signal to the response data signal. Here again, the added

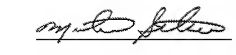
noise signal is dependent on the physics of the noise generator and as such indiscernible to an attacker.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-13 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Mike Belk, Esq., Intellectual Property Counsel, Philips Electronics North America, at 914-945-6000.

Respectfully submitted,



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